REMARKS

Status of Prosecution

Applicant filed the original application on April 5, 2001. The Examiner mailed a first, nonfinal Office Action on September 24, 2004. A Response to that Office Action was filed. The Examiner mailed a second, nonfinal Office Action March 24, 2005. The remarks herein are in response to the second Office Action. Applicant requests reconsideration and withdrawal of the rejections raised in the second Office Action. Claims 1 through 20 are pending.

Claim Rejections

Rejection Under 35 U.S.C. §103

The Examiner rejected claims 1-20 under 35 U.S.C. § 103(a) as unpatentable over Jones et al. (U.S. Patent No. 6,088,800) ("Jones") in view of King (U.S. Patent No. 6,212,576) ("King"). The rejection is respectfully traversed. Applicant submits that the differences between the subject matter sought to be patented and the references cited by the Examiner are not such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

As succinctly stated in the MPEP, to establish a *prima facie* case of obviousness, three basic criteria must be satisfied:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure.

MPEP §706.02(j) (*citing In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991)).

> To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

MPEP §706.02(j) (*quoting Ex parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Inter. 1985)).

Regarding independent claim 1, the Examiner stated that Jones teaches all of the elements of claim 1 except, "Jones et al. does not teach a digital signal processor." Office Action, page 2, ¶ 3. However, claim 1 does not include the limitation of a "digital signal processor." Dependent claim 4, which depends directly from claim 1, does state that the "high performance processor further comprises a digital signal processor." However, the high performance processor of claim 1 is not limited to a digital signal processor because dependent claims by definition further limit the scope of the independent claim from which they depend.

Regardless of this distinction, Jones does not teach the three elements of claim 1 as suggested by the Examiner. Jones describes an "encryption chip" (see Fig. 2) having an "encryption/decryption *pipeline*. . . made up of a plurality of processing elements 37 arranged in a linear array, each containing an instruction memory, a register file, an ALU, local and shared data memory, and control circuitry." Jones, col. 6, ll. 7-13 (emphasis added).

Jones' encryption chip lacks the "first processor operating a software application having a multi-layer protocol as well as "a high performance processor configured to operate one layer of the multi-layer protocol according to a command from the first processor," as claimed by Applicant. Jones also lacks the "memory accessible to each of the first processor and the high performance processor for passing commands and data between the first processor and the high performance processor" as claimed by Applicant.

In rejecting claim 1 over Jones, it appears that the Examiner cited the "processing element(s)" and/or the "control CPU" of Jones as teaching the first and high performance processors of claim 1 – although it is not entirely clear from the cited text – and the memory elements of the "processing elements" of Jones as teaching the memory element of claim 1.

Each processing element ("PE") 37 in Jones:

> consists of an ALU 56 operating on 32-bit words from a register file 58 made up of 8-16 32 bit registers. The register file 58 and ALU 56 *are controlled by a control unit 60 which decodes instructions from a processing element instruction memory 62.* Each processing element instruction memory stores at least one round of an encryption algorithm, where a round is defined as a sequence of instructions in an encryption algorithm.

Jones, col. 7, ll. 17-25, and Fig. 3 (emphasis added). There is *no distinction* from one processing element in Jones to the next. One processing element is *not* a "first processor operating a software application having a multi-layer protocol" while another is "a high performance processor configured to operate one layer of the multi-layer protocol according to a command from the first." All of the processing elements in the pipeline are identical, where each processing element implements a round of an encryption code algorithm. Jones, col. 6, ll. 44-52.

No commands are passed from one processing element to another via a memory, such as in claim 1, "accessible to each of the first processor and the high performance processor." The register file and ALU of each of Jones' processing elements are controlled by a control unit local to each processing element which obtains its instructions from an instruction memory, also *local* to each processing element. See also, Jones, Fig. 3.

The Examiner cited Jones, col. 6, ll. 30-43, for teaching "a high performance processor configured to operate one layer of the multi-layer protocol according to a command from the first processor." Office Action, page 2, ¶ 3. However, lines 30-43 of Jones describe a "public key (PK) core processor 46 ... connected to the control CPU 52." Jones, col. 6, ll. 32-33. The

control CPU 52 described by Jones, merely "synchronizes the operations of the encryption pipeline processors." Jones, col. 6, ll. 26-28. "Furthermore, to allow processing of algorithms which utilize very wide operands such as public-key encryption algorithms, a public-key (PK) core processor 46 is connected to the control CPU 52." Jones, col. 6, ll. 29-33. "Other instructions necessary for implementing PK algorithms can be executed within the control CPU 52." Jones, col. 6, ll. 41-43. In other words the CPU 52 and associated PK core processor certainly are *not* configured to operate one layer of the multi-layer protocol according to a command from a first processor, as claimed by Applicant in claim 1. The Examiner pointed to column 6, lines 12-29 of Jones as teaching the "first processor" element of claim 1. These lines describe the pipeline of processing elements 37.

Then, the Examiner cited Jones, column 6, lines 3-18 as teaching the shared memory element of claim 1. However, these lines describe the contents of each "processing element" of Jones in the pipeline. The only reference to memory in this portion of Jones is in column 6, lines 10-13 where it states, "the pipeline is made up of a plurality of processing elements 37 arranged in a linear array, each containing an instruction memory, a register file, an ALU, local and shared data memory, and control circuitry." The local and shared data memories of each processing element of Jones do not pass commands and data between a first processor and a high performance processor as claimed in claim 1. The local and shared data memory of each processing element (elements 64, 66, and 68 of Jones, Fig. 3 respectively) function to serve the local processing element and those immediately adjacent to it in the pipeline. "The [shared] memories 66 and 68 of a processing element are dual port SRAMs and are shared with the PE of the previous and next pipe stage, respectively." Jones, col. 7, ll. 40-42.

King, column 2, lines 21-26, cited as teaching a "multi-layer protocol high performance processor comprising a digital signal processor" (Office Action, page 2, ¶ 3), are a discussion of a prior art GSM transceiver that includes a digital signal processor. Neither Jones nor King, alone or in combination, teach or suggest the elements recited in claim 1. It would require quite

a leap of impermissible hindsight to see Applicant's invention in either or both of these references.

The obviousness rejection of claim 1 by the Examiner is unsupported by the cited art and should be withdrawn. As independent claim 1 is distinguished over Jones and King, dependent claims 2-6 are similarly distinguished.

Regarding independent claim 7, the Examiner cited Jones, column 7, lines 39-64 as teaching the "high performance processor coupled to the memory and operating a second portion of the predetermined one of the security protocols" element of claim 7. However, no mention of a high performance processor is made anywhere. As stated above, all of the processing elements of Jones are identical, none of which are high performance. Each of the processing elements in the pipeline implements *a round* of an encryption code algorithm. Jones, col. 6, ll. 44-52. Each processing element ("PE") 37 in Jones "consists of an ALU 56 operating on 32-bit words from a register file 58 made up of 8-16 32 bit registers." Jones, col. 7, ll. 18-20. The Examiner cited Jones alone for the rejection of claim 7. None of the basic criteria for an obviousness rejection have been met by reference to Jones. The obviousness rejection of claim 7 is unsupported by the cited art and should be withdrawn. As independent claim 7 is distinguished over Jones, dependent claims 8-11 are similarly distinguished.

Regarding independent claim 12, the Examiner cited Jones, column 17, lines 7-12 as teaching the "one or more application program interfaces. . ." element of claim 12. Jones does not have such interfaces because Jones describes only a pipeline of processing elements, each of which implements *a round* of an encryption code algorithm. Jones, col. 6, ll. 44-52. Lines 7-12 of column 17 in Jones describe the expansion operation of a DES (data encryption standard) encryption routine, which has nothing to do with "one or more application program interfaces operated by the first processor core for interfacing between the security services protocol and the second processor core." The Examiner cited Jones alone for the rejection of claim 12. None of the basic criteria set forth above for an obviousness rejection have been met by reference to Jones. The obviousness rejection of claim 12 is unsupported by the cited art and should be

withdrawn. As independent claim 12 is distinguished over Jones, dependent claims 13-14 are similarly distinguished.

Regarding independent claim 15, the Examiner cited Jones, column 6, lines 44-67, and column 7, lines 1-14 as teaching the partitioning, distributing, and performing steps of the claimed method. Again, as discussed in detail above, Jones does not teach, suggest, or describe partitioning a function of a multi-layer protocol over to a high performance processor. The cited text of Jones describes the processor element pipeline that "implements the code for each round of a secret key algorithm." Jones, col. 6, ll. 44-45. Jones, column 7, lines 25-38, cited by the Examiner as teaching the returning step of the claimed method, actually describe the local, shared, and global memories of the Jones encryption chip. Again, Jones makes no mention of "returning a result of the distributed function from the high performance processor via the shared memory."

The obviousness rejection of claim 15 is unsupported by the cited art and should be withdrawn. As independent claim 15 is distinguished over Jones, dependent claims 16-20 are similarly distinguished.

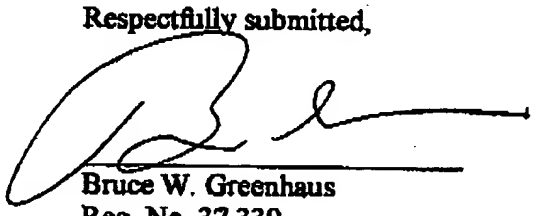
Conclusion

For the reasons set forth above, Applicant respectfully requests reconsideration and withdrawal of the foregoing rejections.

Applicant respectfully submits that the actions taken by Applicant do not raise new issues that would require further consideration or a new search and do not raise new matter.

Applicant asserts that this Response is complete as contemplated in 37 CFR §1.111, that claims 1-20 are patentable for the reasons set forth above, and that the Application is now in condition for allowance. Accordingly, Applicant respectfully requests an early notice of allowance.

Respectfully submitted,



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